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DESIGN OF TERNARY LOGIC ARITHMATIC CIRCUITS USING CARBON NANO-TUBE FIELD EFFECT TRANSITORS

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ABSTRACT

This paper presents a design of ternary arithmetic circuits including half-adder, full-adder and 1-bit comparator using Carbon Nano-Tube field effect transistors (CNTFET). The CNTFET has unique characteristics of behavior according to its arrangement of atoms. Threshold voltage of CNTFETs can vary by changing its diameter and also one intermediate state between two normal stable ON and OFF states introduced for multi-valued logic computation. Moreover ternary logic is a promising alternative to the conventional binary logic design technique, since it is possible to produce three states (TRUE, FALSE & UNKNOWN), and also reduces the number of interconnects and chip area and increases efficiency. Novel circuit design of half-adder and comparator based on ternary logic CNTFETs is proposed in this paper, where increased number of states in CNTFETs will eventually increase the number of bit handling capacity in the device.

Keywords:- Carbon Nano-Tube Field Effect Transistor (CNTFET), Multi Valued Logic (MVL), Half-Adder, Full-Adder, Comparator.

INTRODUCTION

Traditionally, digital computation is performed on two-valued logic, i.e., there are only two possible values (0 or 1, otherwise known as true or false) in the Boolean space. Multiple-valued logic (MVL) replaces the classical Boolean characterization of variables with either finitely or infinitely many values such as ternary logic, according to Lin et al (2016) or fuzzy logic, according to Araki et al (2017). Ternary logic is a three-valued logic which has attracted considerable interest due to its potential advantages over binary logic for designing digital systems. Antoniou et al (2016) provided an illustration which showed that it is possible for ternary logic to achieve simplicity and energy efficiency in digital design since the logic reduces the complexity of interconnects and chip area. Furthermore, serial and serial-parallel arithmetic operations can be carried out faster if the ternary logic is employed.

There are two kinds of MVL circuits based on Metal Oxide Semiconductor (MOS) technology, namely the current-mode MVL circuits and the voltage mode MVL circuits. Voltage-mode MVL circuits have been achieved in multi threshold Complementary Metal Oxide Semiconductor (CMOS) design, as proven by Yasuda et al (2018). However, Appenzeller (2019) opined that Carbon Nano-Tube Field Effect Transistor (CNTFET) could provide a durable alternative to the bulk silicon transistor for low-power and high-

performance design due to its ballistic transport and low OFF-current properties. A multi threshold CMOS design relies on body effects using different bias voltages to the base or the bulk terminal of the transistors. In a CNTFET, the threshold voltage of the transistor is determined by the diameter of the CNT. Therefore, a multi threshold design can be accomplished by employing CNTs with different diameters (and, therefore, chirality) in the CNTFETs.

The design of ternary arithmetic circuits such as half adder, full adder, comparator are designed in this paper by using basic ternary logic gates. This is because the ternary logic gates provide a good platform for decoding circuit blocks since it requires less number of logic gates while binary logic gates provide a good platform for fast computation as observed by Akturk et al (2017).

REVIEW OF TERNARY LOGIC

Ternary logic functions are defined as those functions having significance of a third value introduced to the binary logic. In this paper, 0, 1, and 2 denote the ternary values to represent false, undefined, and true, respectively. Any n variable $\{X_1, \ldots, X_n\}$ ternary function f(X) is defined as a logic function mapping $\{0, 1, 2\}^n$ to $\{0, 1, 2\}$, where $X = \{X_1, \ldots, X_n\}$. The basic operations of ternary logic can therefore be defined, according to Hashempour et al (2018), by Equation (1), where $X_i, X_j = \{0, 1, 2\}$:

$$X_i + X_j = max\{X_i, X_j\}$$
$$X_i \bullet X_j = min\{X_i, X_j\} \quad (1)$$
$$\overline{X_i} = 2 - X_i$$

where − denotes the arithmetic subtraction, the operations +, •, and bar are referred to as the OR, AND, and NOT in ternary logic, respectively. The fundamental gates in the design of digital systems are the inverter, the NOR gate, and the NAND gate. The assumed logic symbols are shown in Table 1. The ternary gates are designed according to the convention defined in Equation (1).

Table 1: Logic Symbols

Voltage Level	Logic Value
0	0
½V_{dd}	1
V_{dd}	2

A. Ternary Inverter

A general ternary inverter is an operator (gate) with one input x, and three outputs (denoted by y0, y1, and y2) such that

$$y0 = C0(x) = \begin{cases} 2, \text{ if } x = 0 \\ 0, \text{ if } x \neq 0 \end{cases}$$
$$y1 = C1(x) = \bar{x} = 2 - x \quad (2)$$
$$y2 = C2(x) = \begin{cases} 2, \text{ if } x \neq 2 \\ 0, \text{ if } x = 2 \end{cases}$$

Therefore, the implementation of ternary inverter requires three inverters, which are a negative ternary inverter (NTI), a standard ternary inverter (STI), and a positive ternary inverter (PTI), knowing that y0, y1, and y2 are the outputs as expressed in Equation (2), Raychowdhury et al (2018). The truth table of the three ternary inverters is shown in Table 2.

Table 2: Truth Table of Ternary Inverters

Input X	STI	PTI	NTI
0	2	2	2
1	1	2	0
2	0	0	0

B. Ternary NOR and NAND Gates

The ternary NAND and NOR are two multiple entry operators used in ternary logic. The functions of the two-entry ternary NAND and NOR gates are defined, as postulated by Lin et al (2017) by Equations (3) and (4), respectively.

$$Y_{nand} = \overline{\min\{X_1, X_2\}} \quad (3)$$
$$Y_{nor} = \overline{\max\{X_1, X_2\}} \quad (4)$$

The truth table of ternary NAND and NOR gates is shown in Table 3.

Table 3: Truth Table of NAND and NOR gates

Input X_1	Input X_2	Y_{NAND}	Y_{NOR}
0	0	2	2
1	0	2	1
2	0	2	0
0	1	2	1
1	1	1	1
2	1	1	0
0	2	2	0
1	2	1	0
2	2	0	0

CARBON NANOTUBE FET

CNTFETs utilize semiconducting single-wall CNTs to assemble electronic devices. A single-wall CNT (SWCNT) consists of one cylinder only, and the simple manufacturing process of this device makes it very promising for alternative to today's MOSFET. An SWCNT can act as either a conductor or a semiconductor, depending on the angle of the atom arrangement along the tube. This is referred to as the chirality vector and is represented by the integer pair (n,m). A simple method to determine if a CNT is metallic or semiconducting is to consider its indexes (n,m): the nanotube is metallic if $n = m$ or $n - m = 3i$, where i is an integer. Otherwise, the tube is semiconducting. From Jimmy et al's work (2018), it was discovered that the diameter of the CNT can be calculated based on Equation (5).

$$D_{cnt} = \frac{\sqrt{3}a0}{\pi}\sqrt{n^2 + m^2 + nm} \qquad (5)$$

where a0 (= 0.142 nm) is the interatomic distance between each carbon atom and its neighbour. Zhang et al (2019) came up with a schematic diagram of CNTFET shown in Figure 1. Similar to the traditional silicon device, the CNTFET also has four terminals. As shown in Figure 1, undoped semiconducting nanotubes are placed under the gate as channel region, while heavily doped CNT segments are placed between the gate and the source/drain to allow for a low series resistance in the ON-state. As the gate potential increases, the device is electrostatically turned on or off via the gate.

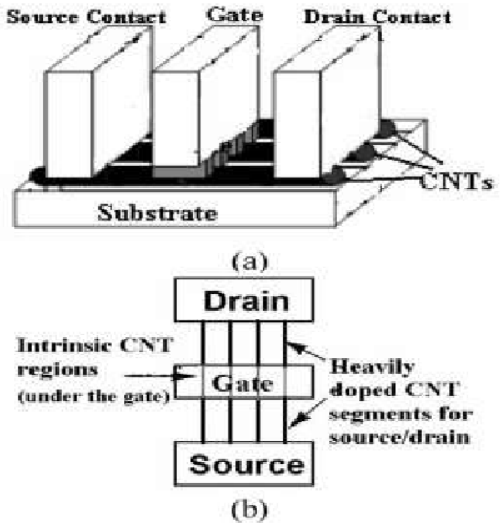

Figure 1: Basic structure of CNTFET

The I-V characteristics of the CNTFET are similar to those of MOSFET. The threshold voltage is defined as the voltage required to turn ON transistor. The threshold voltage of the intrinsic CNT channel can be approximated to the first order as the half band gap that is an inverse function of the diameter, according to Lin et al (2018), i.e.

$$V_{th} \approx \frac{E_g}{2e} = \frac{\sqrt{3}}{3}\frac{aV\pi}{eD_{cnt}} \quad (6)$$

where a = 2.49 Å is the carbon to carbon atom distance, Vπ =3.033 eV is the carbon π-π bond energy in the tight bonding model, e is the unit electron charge, and DCNT is the CNT diameter. As DCNT of a (19, 0) CNT is 1.487 nm, the threshold voltage of a CNTFET using (19, 0) CNTs in the channel is 0.293 V from Equation (6). Simulation results have confirmed the correctness of this threshold voltage. As the chirality vector changes, the threshold voltage of the CNTFET will also change. Assume that m in the chirality vector is always zero, then the ratio of the threshold voltages of two CNTFETs with different chirality vectors will be:

$$\frac{V_{th1}}{V_{th2}} = \frac{D_{cnt2}}{D_{cnt1}} = \frac{n2}{n1} \quad (7)$$

Equation (7) shows that the threshold voltage of a CNTFET is inversely proportional to the chirality vector of the CNT. For example, the threshold voltage of a CNTFET using (13, 0) CNTs is 0.428 V, compared to a (19, 0) CNTFET with a threshold voltage of 0.293 V.

ARITHMETIC CIRCUITS BASED ON CNTFET

A. 1-Bit Comparator

A 1-bit comparator compares two input bits which are in ternary logic and gives three outputs based on the comparison between these two three valued input signals and three outputs are: A > B, A = B, and A < B in the comparator circuits. Based on the relation between two inputs (A and B), corresponding output becomes high and others remain low. The truth table of the ternary logic 1-bit comparator is shown in Table 4. The logic block diagram and the input/output waveform of a ternary comparator obtained in the Matlab environment are shown in Figures 2 and 3 respectively.

Table 4: Truth Table of Ternary 1-bit Comparator

A	B	A<B	A=B	A>B
0	0	0	2	0
0	1	2	0	0
0	2	2	0	0
1	0	0	0	2
1	1	0	2	0
1	2	2	0	0
2	0	0	0	2
2	1	0	0	2
2	2	0	2	0

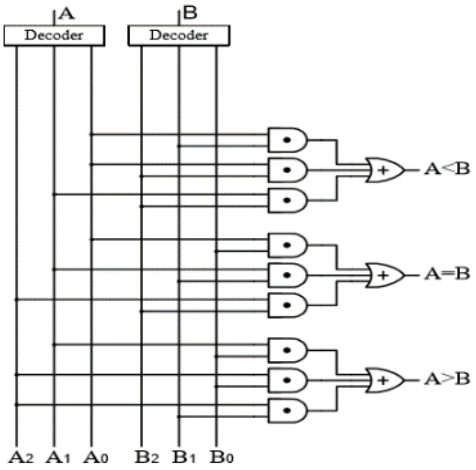

Figure 2: Ternary 1-bit Comparator

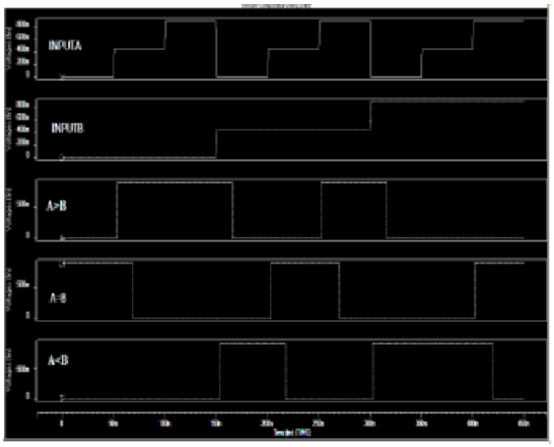

Figure 3: Simulated result of Ternary 1-bit Comparator

B. Half Adder

A ternary half adder adds two ternary inputs and gives output as ternary sum bits and carry bits. The truth table of a ternary half adder is shown in Table 5. The logic function for sum and carry bit can be derived from Equation (8), as stated by Araki et al (2017).

$$Sum = A_2B_0 + A_1B_1 + A_0B_2 + 1 \bullet (A_1B_0 + A_0B_1 + A_2B_2)$$
$$Carry = 1 \bullet (A_2B_1 + A_2B_2 + A_1B_2) \quad (8)$$

Table 5: Truth Table of Ternary Half-Adder

A	B	SUM	CARRY
0	0	0	0
0	1	1	0

0	2	2	0
1	0	1	0
1	1	2	0
1	2	0	1
2	0	2	0
2	1	0	1
2	2	1	1

In equation (8), A_k and B_k are the outputs from the ternary decoder corresponding to the inputs A and B shown in Figure 4. The schematic diagram of a ternary half adder is shown in Figure 4 which consists of T-Decoder, two input T-AND gates, three input T-OR gates and T-Buffers.

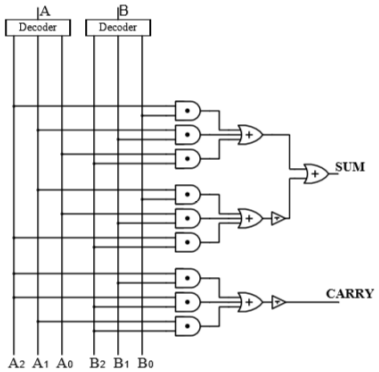

Figure 4: Ternary Half-Adder

C. Full Adder

A 1-bit ternary full adder adds two ternary numbers and previously calculated carry which here denoted as C_{in}. This circuit produces a 2-bit output sum represented by the signals C_{out} and SUM. A ternary full adder can be implemented by cascading two ternary half adder circuits. Figure 5 shows the ternary full adder block diagram using two ternary half adders block. Here the first half adder adds 2 input bits A and B.

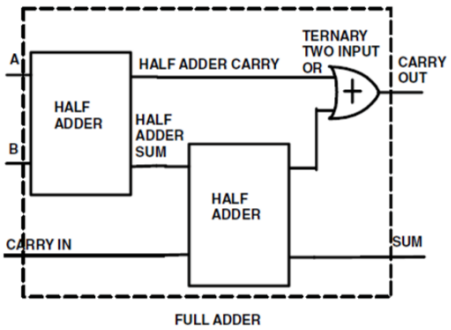

Figure 5: Ternary Full-Adder

The following half adder adds the sum output of A and B inputs with past carry (C_{in}) and generates sum bit and one carry bit in its output. The final carry bit (C_{out}) is generated by the OR operation between the two carry bits generated from the two stages (first half adder and the second half adder). Table 6 shows the truth table of the Ternary fill-adder and Figure 6 shows the waveforms of the designed ternary full adder circuit.

Table 6: Truth Table of Ternary Full-Adder

A	B	C_{in}	SUM	C_{out}
0	0	0	0	0
0	0	1	1	0
0	0	2	2	0
0	1	0	1	0
0	1	1	2	0
0	1	2	0	1
0	2	0	2	0
0	2	1	0	1
0	2	2	1	1
1	0	0	1	0
1	0	1	2	0
1	0	2	0	1
1	1	0	2	0
1	1	1	0	1
1	1	2	1	1
1	2	0	0	1
1	2	1	1	1
1	2	2	2	1
2	0	0	2	0
2	0	1	0	1
2	0	2	1	1
2	1	0	0	1
2	1	1	1	1
2	1	2	2	1
2	2	0	1	1
2	2	1	2	1
2	2	2	0	2

SIMULATION RESULTS

Figures 5, 6, and 7 show the simulation results of proposed ternary Arithmetic circuits of ternary 1-bit comparator, ternary half-adder and ternary full-adder. From the simulated results, it could be seen clearly that the proposed ternary arithmetic designs work, based on Carbon Nano-Tube Field Effect Transistor model, by producing the expected and appropriate outputs.

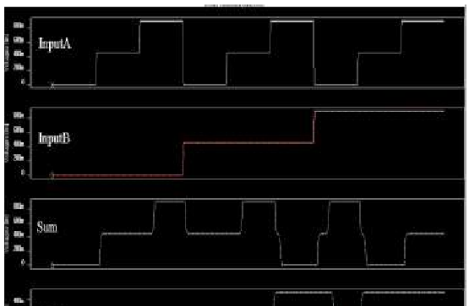

Figure 6: Simulated result of Ternary Half-Adder

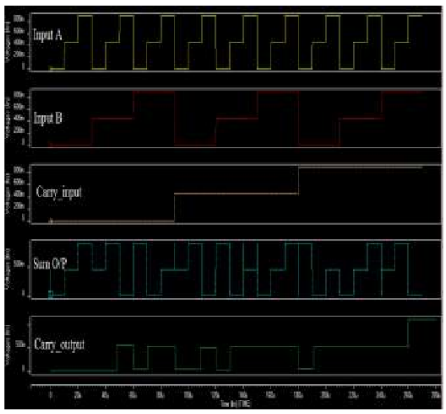

Figure 7: Simulated result of Ternary Full-Adder

CONCLUSION

This paper presented the design of ternary logic arithmetic circuits based on Carbon Nano-Tube Field Effect Transistor (CNTFET). This is the future technology to the predominant Complementary Metal-Oxide Semiconductor (CMOS) Technology. The major drawback of traditional CMOS technology is scaling of its size, which the proposed work takes care of. Furthermore, less power dissipation was observed in the CNTFET-based ternary logic circuits than the CMOS technology. The threshold voltage of CNTFET is depends on its diameter, the threshold voltage could be controlled easily and better than in CMOS. With these great technological advantages it could be seen that, CNTFET-based ternary circuit design is a promising circuit element in Multi-valued Logic (MVL) circuits in the near future.

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